REMARKS

In numbered Section 1 of the Office Action, the Examiner has imposed a requirement for new drawings based on an objection to the drawings filed November 3, 2003. In responding to the Notice to File Missing Parts, response filed April 5, 2004, Applicant's submitted a set of five sheets of formal drawings including Figs. 1A through 5. Applicant's assume that the Examiner's Section 1 objection to the drawings is due to oversight in view of the fact that the formal drawings should be part of the application file. In the event that they have gotten separated from the application file and cannot be located, Applicant's are prepared to submit a replacement set.

Relative to the objection to claim 1, numbered Section 2, Applicant's copies of claim 1 do not include the quotation noted by the Examiner. However, in an attempt to be responsive claim 1 has been amended.

Applicant's have very carefully considered the Examiner's substantive rejections pursuant to 35 U.S.C. §102 and 103. As described below, none of claims 1-4 are anticipated by Deutsch et al. None of the remaining rejected claims are obvious and unpatentable in view of the teaching of Deutsch et al.

Deutsch et al. discloses a time based testing system which tests installed and operational units such as the drivers 12. For example, in Deutsch et al., periodically, see Fig. 5A thereof and flow diagram, Fig. 6A thereof, test installed operational units, for example, when a vehicle is operating. As described by Deutsch et al.:

> "However, the controller 11 does differ from those prior controllers, which include controllers that produce primary modulation and submodulation pairs of controller signals, in that within each primary modulation period T, there exists separate time intervals t_A and t_B. During these time periods t_A and t_B ... During these time periods t_A and t_B each of the driver stages 1-11 [drivers 12] will be tested for faults while preferably each of the driver stages is forced into a common effective on or off state, respectively." (Col. 5, lines 59-68 Deutsch et al.)

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Unlike the system and teachings of Deutsch et al., a system which embodies the present invention is situational based. Where an electrical unit is initially coupled to the system, initial installation testing is effected. This is not time based, but is triggered by installation of the respective electrical unit.

None of claims 1-4 are anticipated. The Examiner has argued that claims 1-4 are anticipated by Deutsch et al. in view of the fact that Deutsch et al. includes and teaches "a second mode of operation, activated for a limited, predetermined time interval, upon being coupled to the medium" (page 3, Office Action)

The above quoted phraseology is an inaccurate representation of the teaching of Deutsch et al. To the contrary, Deutsch et al. carries out only timing based testing. This is extensively described starting on Col. 14, line 22 and extending at least through Col. 16, line 67.

In the above regard, Deutsch et al. have stated:

> "After the background task subroutine 62, a decision block 73 inquires if it is time for performing the off tests during the time t_B. If so, a decision block 74 asks if the fault flag has been set indicating that a fault has been detected and not reset....If the fault flag is not set, decision block 74 then proceeds to process block 75 which forces the submodulation signals SM for all of the drivers into an off state by preventing any of the signals SM going to the drivers from having positive going pulses during this time." (Col. 14, lines 22-35)

The above describes the so-called t_B test sequence of Deutsch et al. Deutsch et al. further states:

> "What has been described so far implements the procedures for conducting the off time tests during the time periods t_B for each of the driver stages 1-11. If the decision block 73 determines that it is not time for the off testing of the driver stages, decision block 101 inquires if it is time for performing the on tests for the driver stages during the time period t_4. If

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not, control returns to the initial terminal 61. If it is time for conducting the
on tests of the driver stages, control passes to the process block 102 which
results in forcing the submodulation signals constantly on for those driver
stages which are intended to be on by virtue of the primary modulation
signal having a high logic state." (Col. 16, lines 37-49)

As the above two paragraphs make clear, Deutsch et al. is timed based in response to whether the appropriate time is at hand for either the t_B or t_A type testing.

In contradistinction to the time based testing of Deutsch et al., all of claims 1-4 require:

"a second mode of operation, activated for a limited, predetermined
time interval, upon being coupled to the medium" (claims 1-4)

The time based test initiation sequence and process of Deutsch et al. is thus different from and does not anticipate any of claims 1-4 for at least the above reasons.

Dependent claims 5-16 all depend from claim 1. Those claims are allowable in view of the fact that, as described above, Deutsch et al. is a time based testing system. Deutsch et al. includes no motivation, suggestion or disclosure which would cause one of ordinary skill in the art to modify that system so as to make the structure any of claims 5-16 obvious for at least the same reasons that claims 1-4 are not anticipated by Deutsch et al. Simply put, Deutsch et al. discloses a system which has a fundamentally different operating principle than the structures of claims 5-16 for the reasons set forth above.

In the Office Action, the Examiner failed to address independent claim 17. Dependent claims 18-20 have been rejected as obvious and unpatentable in view of Deutsch et al. However, it is quite clear that the structure of Deutsch et al. not only is quite different from, it does not motivate, suggest or teach one of ordinary skill in the art how to modify that structure so as to make any of claims 17-19 obvious.

For example, Fig. 2 of Deutsch et al. discloses the structure of the driver units 12. The driver units 12 have a plurality of signal input output ports labeled "primary modulation", "submodulation" and "to multiplexer 15". Thus, the units 12 include a plurality of separate input and output ports. Those three ports are signal ports and do not provide electrical energy for the unit 12. Electrical energy for the unit 12 is provided from a source labeled "B+" within that unit.

By way of contrast, all of claims 17-20 include:

"a port for receipt of electrical energy and control signals"

As noted above, there is no motivation, suggestion or teaching in Deutsch et al. which would cause one of ordinary skill in the art to modify that structure to make any of claims 17-20 obvious and unpatentable. Similar comments apply to Deutsch et al.'s controller 11. That controller includes a plurality of signal ports and separate sources of electrical energy, see Fig. 1 thereof.

Thus, for at least the above reasons, all of claims 17-20 are allowable.

In attempting to establish a rationale for rejecting method claims 21-23 and 25, the Examiner has merely set forth a rejection in a cursory fashion without addressing the various steps set forth in those claims. For example, and without limitation all of those claims require:

"providing a first, non-alarm indicating signal sequence; energizing a unit being installed in the system and coupling the first sequence thereto; providing at least one of an audible or visual indicator indicative of normal operation of the unit for a predetermined period of time during which the first sequence is coupled to the unit." (claims 21-23 and 25)

As described above, Deutsch et al. disclose and teach a time based diagnostic system which repetitively carries out test sequences of all of the units 12. This is quite unlike the claimed methodology for at least the above stated reasons.

For all of the above reasons the pending claims are allowable and allowance of the application is respectfully requested.

Respectfully submitted,

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